Session 29 Overview

Power Management and Distribution

Chair: Atila Alvandpour, Linköping University, Sweden

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Design of power management and distribution is getting significantly more difficult for each new CMOS technology node. Power management and distribution ensures robust and consistent operating voltages to complex ICs independent of their operating conditions and changes to their operational environment (for example, changes to clock frequency). Furthermore effective and systematic control of leakage currents is becoming one of the main challenges especially for circuits used in portable applications.

The eight papers in this session present the current state-of-the-art in power distribution and management, on-chip measurements, voltage-domain stacking for high voltage I/O, and ESD protection to power pins.

In Paper 29.1, spatially-resolved imaging of microprocessor power is shown to be a critical tool for the development of multi-core processors. In Paper 29.2, an on-chip linear regulator for biasing DC-DC converters is introduced. For supporting local stable operating voltages and improved frequency, high-K MIM decoupling capacitors are implemented in Paper 29.3.

For complex and heterogeneous single-chip multi-CPU processors, multiple power domains need to be implemented for controlling both the leakage currents and performance. In Paper 29.4 and Paper 29.5, techniques and implementations of a 20 power domain multi-core CPU is discussed for portable 3G/GSM applications.

Systematic fully-integrated signal integrity self-test with analog monitors and digital test-compatible scan chains is introduced in Paper 29.6 for monitoring signal integrity and performance parameters of the chip. In Paper 29.7 an ESD protection design for 1.2V/2.5V mixed-voltage I/O interfaces by using high-voltage-tolerant power-rail ESD clamp circuit realized with low-voltage devices is presented.

When a high-performance processor is changing its operating clock frequency it can introduce large voltage disturbances in power rails. In Paper 29.8, a circuit is proposed which controls the frequency ramp between initial and final operating frequency by periodically masking clock pulses to change incrementally the average clock frequency.

29.1 Power Distribution Measurements of the Dual Core PowerPC™ 970MP Microprocessor **1:30 PM**
H. Hamann, IBM, Yorktown Heights, NY

Spatially-resolved imaging of microprocessor power (SIMP) is shown to be a critical tool for measuring temperature and power distributions of a microprocessor under full operating conditions. In this paper, the SIMP technique is applied to the dual-core PowerPC™ 970MP microprocessor.

29.2 A Linear Regulator with Fast Digital Control for Biasing Integrated DC-to-DC Converters **2:00 PM**
P. Hazucha, Intel, Hillsboro, OR

A high-voltage-tolerant 2.4 to 1.2V push-pull linear regulator with 1A output, 288ps response time, and 97.5% current efficiency for biasing integrated dc-to-dc converters is introduced. The regulator occupies 0.03mm^2 in 90nm CMOS and achieves 33A/mm^2 current density. Digital control with a flash ADC and a digital-to-current converter improve speed-power performance by 3X.

29.3 Increasing Microprocessor Speed by Massive Application of On-Die High-K MIM Decoupling Capacitors **2:30 PM**
H. Sánchez, Freescale Semiconductor, Austin, TX

A 90nm SOI microprocessor with massive application of high-K MIM decoupling capacitor modules is proven to increase the maximum frequency of the processor by close to 10%. Simulations predict reduced power supply noise leading to improvements in Fmax by close to the equivalent of a transistor node increase. Simulations of applying MIM decoupling capacitors to high-speed I/O and PLL circuits show that they can further enhance performance and area requirements for these critical circuits in advanced technologies.

29.4 Hierarchical Power Distribution with 20 Power Domains in 90nm Low-Power Multi-CPU Processor **3:15 PM**
Y. Kanno, Hitachi, Tokyo, Japan

Hierarchical power distribution using a power tree is developed. It supports fine-grained power gating with dozens of power domains like fine-grained clock gating and effectively reduces leakage currents for 1-million-gate power domains to 1/4000 in multi-CPU processors with minimal area overhead. This paper demonstrates the integration of 20 power domains in a 90nm single-chip 3G cellular phone processor.

29.5 A Power Management Scheme Controlling 20 Power Domains for a Single-Chip Mobile Processor **3:30 PM**
T. Hattori, Renesas Technology, Tokyo, Japan

A power-management scheme for a single-chip multi-CPU processor uses 20 power domains. The scheme enables the minimization of leakage currents in each opearating mode: 299μA in paging operation and 7μA in stand-by. The techniques for controlling and implementing power domains are also described.

29.6 A Signal-Integrity Self-Test Concept for Debugging Nanometer CMOS ICs **3:45 PM**
V. Petrescu, Philips, Eindhoven, The Netherlands

A fully integrated signal-integrity self-test concept is implemented in a 90nm CMOS process. The outputs of different analog monitors are locally converted to digital form and then transported through a test-compatible scan chain. The temperature monitor has 4b resolution. The supply-noise monitor detects 10ps-wide pulses of 20mV. The total area overhead is <0.1%.

29.7 ESD Protection for Mixed-Voltage I/O in Low-Voltage Thin-Oxide CMOS **4:15 PM**
W-J., Chang, National Chiao-Tung University, Hsin-Chu, Taiwan

An ESD protection design for 1.2V/2.5V mixed-voltage I/O interfaces is discussed. A high-voltage-tolerant power-rail ESD clamp circuit is used; it is realized with low-voltage devices in a 0.13μm CMOS process. The four-mode ESD stresses on the mixed-voltage I/O pad and the whole-chip pin-to-pin ESD protection can be discharged by the proposed ESD protection scheme.

29.8 A Circuit for Reducing Large Transient Current Effects on a Processor Power Grid **4:45 PM**
E. Hailu, IBM, Austin, TX

A circuit that reduces power supply transients by controlling the frequency ramp between the initial and final operating frequencies of a microprocessor is presented. This is accomplished by periodically 'masking' clock pulses to incrementally increase or decrease the average clock frequency until the final clock frequency is reached. This circuit is implemented in a 90nm partially-depleted SOI technology.